

## WEST Search History





DATE: Monday, March 21, 2005

<u>Hide?</u>	<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>
	<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>		
<input type="checkbox"/>	L82	L72 and L81	6
<input type="checkbox"/>	L81	(712/23).ccls.	691
<input type="checkbox"/>	L80	L48 and L77	1
<input type="checkbox"/>	L79	L32 and L77	1
<input type="checkbox"/>	L78	L72 and L77	3
<input type="checkbox"/>	L77	(712/241).ccls.	235
<input type="checkbox"/>	L76	L53 and L72	0
<input type="checkbox"/>	L75	L53 and L74	0
<input type="checkbox"/>	L74	L21 and L72	974
<input type="checkbox"/>	L73	L48 and L72	19
<input type="checkbox"/>	L72	packet switch\$3	17799
<input type="checkbox"/>	L71	sun.as. and treat.xp. and L21	8
<input type="checkbox"/>	L70	L21 same L69	31
<input type="checkbox"/>	L69	instruction block\$1	1864
<input type="checkbox"/>	L68	L21 and L66	5
<input type="checkbox"/>	L67	packet\$1 and L66	13
<input type="checkbox"/>	L66	decoupled processor\$1	56
<input type="checkbox"/>	L65	L64 adj processor\$1	5
<input type="checkbox"/>	L64	non-blocking or nonblocking	6386
<input type="checkbox"/>	L63	mon-blocking or nonblocking	1219
<input type="checkbox"/>	L62	L21 with L48	17
<input type="checkbox"/>	L61	L21 adj processor	629
<input type="checkbox"/>	L60	L48 and L53	1
<input type="checkbox"/>	L59	L45 and L53	3
<input type="checkbox"/>	L58	L53 and L57	1
<input type="checkbox"/>	L57	(712/32).ccls.	355
<input type="checkbox"/>	L56	context switch\$3 same L42	29
<input type="checkbox"/>	L55	L42 and L53	1
<input type="checkbox"/>	L54	L32 and L53	0
<input type="checkbox"/>	L53	(712/235).ccls.	171
<input type="checkbox"/>	L52	packet\$1.ti,ab,clm. and L51	8

<input type="checkbox"/>	L51	L48 with (parallel or pipelin\$3)	124
<input type="checkbox"/>	L50	packet\$1.ti,ab,clm. and L48	72
<input type="checkbox"/>	L49	packet.ti,ab,clm. and L48	58
<input type="checkbox"/>	L48	subprocessor\$1 or sub-processor\$1	1025
<input type="checkbox"/>	L47	L21 same L45	28
<input type="checkbox"/>	L46	packet\$1 same L45	16
<input type="checkbox"/>	L45	non-blocking with processor\$1	332
<input type="checkbox"/>	L44	L43 not L41	5
<input type="checkbox"/>	L43	L42 and L36	14
<input type="checkbox"/>	L42	packet with processor\$1	11300
<input type="checkbox"/>	L41	L32 and L36	9
<input type="checkbox"/>	L40	packet\$1 and L35	22
<input type="checkbox"/>	L39	L35 and L38	7
<input type="checkbox"/>	L38	conditional branch\$3	5109
<input type="checkbox"/>	L37	L35 and L36	0
<input type="checkbox"/>	L36	(712/234).ccls.	332
<input type="checkbox"/>	L35	serial processors	97
<input type="checkbox"/>	L34	L21 with L32	24
<input type="checkbox"/>	L33	L21 and L32	151
<input type="checkbox"/>	L32	packet processor\$1	1420
<input type="checkbox"/>	L31	L30 not private branch exchange	33
<input type="checkbox"/>	L30	L28 not L29	44
<input type="checkbox"/>	L29	branch\$3 same L27	5
<input type="checkbox"/>	L28	branch\$3 and L27	49
<input type="checkbox"/>	L27	L21 same L24	221
<input type="checkbox"/>	L26	branch\$3 and L25	453
<input type="checkbox"/>	L25	L21 and L24	2571
<input type="checkbox"/>	L24	decoupled	26329
<input type="checkbox"/>	L23	L21 and L22	4
<input type="checkbox"/>	L22	decoupled architecture	29
<input type="checkbox"/>	L21	multi-threading or multithreading or thread\$1	286029
<input type="checkbox"/>	L20	chained processor\$1	8
<input type="checkbox"/>	L19	L11 and L18	0
<input type="checkbox"/>	L18	L17 with buffer\$1	0
<input type="checkbox"/>	L17	reconfigurable pipeline\$1	86
<input type="checkbox"/>	L16	L12 and L15	2
<input type="checkbox"/>	L15	709/\$.ccls.	34918

<input type="checkbox"/>	L14	router\$1 and L12	17
<input type="checkbox"/>	L13	L11 and L12	2
<input type="checkbox"/>	L12	reservation station\$1	995
<input type="checkbox"/>	L11	internet protocol or tcp	59908
<input type="checkbox"/>	L10	L8 and L9	18
<input type="checkbox"/>	L9	reservation station\$1 with branch\$3	320
<input type="checkbox"/>	L8	internet protocol or ip or tcp	113147
<input type="checkbox"/>	L7	reservation station\$1 and L6	10
<input type="checkbox"/>	L6	(data or network) adj packet\$1	42938
<input type="checkbox"/>	L5	(router\$1 or switch\$2) and L4	76
<input type="checkbox"/>	L4	packet\$1 and reservation station\$1	143
<input type="checkbox"/>	L3	L1 same next instruction	18
<input type="checkbox"/>	L2	pipeline stage\$1 with conditional branch\$3	105
<input type="checkbox"/>	L1	pipeline stage\$1 with branch\$3	483

END OF SEARCH HISTORY